

Q.3.4: Consider a cache with 256 bytes. Word size is 4 bytes and block size is 16 bytes. Show the values in the cache and tag bits after each of the following memory access operations for the two cache organizations: direct mapped and 2-way associative. Also indicate whether the access was a hit or a miss. Specify. The addresses are in hexadecimal representation. Use LRU (least recently used) replacement algorithm whenever needed.

1. Read 0010
2. Read 001C
3. Read 0018
4. Write 0010
5. Read 04B4
6. Read 001C
7. Read 001C
8. Read 0210
9. Read 001C

Solution: http://targetprocess.blogspot.in/2013/11/modern-processor-design-by-john-paul_1.html

Ex. 3.13 Solution : Modern Processor Design by John Paul Shen and Mikko H. Lipasti : Solution Manual

Q.3.13: Consider a processor with 32-bit virtual addresses, 4KB pages and 36-bit physical addresses. Assume memory is byte-addressable (i.e., the 32-bit VA specifies a byte in memory).

L1 instruction cache: 64 Kbytes, 128 byte blocks, 4-way set associative, indexed and tagged with virtual address.

L1 data cache: 32 Kbytes, 64 byte blocks, 2-way set associative, indexed and tagged with physical address, write-back.

4-way set associative TLB with 128 entries in all. Assume the TLB keeps a dirty bit, a reference bit, and 3 permission bits (read, write, execute) for each entry.

Specify the number of offset, index, and tag bits for each of these structures in the table below. Also, compute the total size in number of bit cells for each of the tag and data arrays.

Solution: <http://targetprocess.blogspot.in/2013/11/cs-313-solution-modern-processor-design.html>

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