

FIITJEE Big Bang Edge Test - 2023

for students presently in **Class IX (going to X) (Paper 2)**
SAMPLE PAPER

Time: 3 Hours (1:45 pm – 4:45 pm)

CODE: 910-2

Maximum Marks: 272

Instructions:

Caution: Class, Paper, Code as given above **MUST** be correctly marked on the answer OMR sheet before attempting the paper. Wrong Class, Paper or Code will give wrong results.

1. You are advised to devote 55 Minutes on Section-I, 45 Minutes on Section-II, 40 Minutes on Section-III and 40 Minutes on Section-IV.
2. This Question paper consists of 4 sections. Marking scheme is given in table below:

Section	Subject	Question no.	Marking Scheme for each question	
			Correct answer	Wrong answer
SECTION – I	PHYSICS (PART-A)	1 to 12	+1	0
	CHEMISTRY (PART-B)	13 to 24	+1	0
	MATHEMATICS (PART-C)	25 to 36	+1	0
	BIOLOGY (PART-D)	37 to 48	+1	0
SECTION – II	PHYSICS (PART-A)	49 to 52	+4	-1
	CHEMISTRY (PART-B)	53 to 56	+4	-1
	MATHEMATICS (PART-C)	57 to 60	+4	-1
	BIOLOGY (PART-D)	61 to 68	+4	-1
SECTION – III	PHYSICS (PART-A)	69 to 76	+3	-1
	CHEMISTRY (PART-B)	77 to 84	+3	-1
	BIOLOGY (PART-C)	85 to 92	+3	-1
SECTION – IV	PHYSICS (PART-A)	93 to 97	+3	0
	CHEMISTRY (PART-B)	98 to 102	+3	0
	MATHEMATICS (PART-C)	103 to 107	+3	0
	PHYSICS (PART-D)	108 to 110	+3	0
	CHEMISTRY (PART-E)	111 to 113	+3	0
	MATHEMATICS (PART-F)	114 to 116	+3	0

3. Answers have to be marked on the OMR sheet. The Question Paper contains blank spaces for your rough work. No additional sheets will be provided for rough work.
4. Blank papers, clip boards, log tables, slide rule, calculator, cellular phones, pagers and electronic devices, in any form, are not allowed.
5. Before attempting paper write your OMR Answer Sheet No., Registration Number, Name and Test Centre in the space provided at the bottom of this sheet.
6. See method of marking of bubbles at the back of cover page for question no. 108 to 116.

Note: Please check this Question Paper contains all **116** questions in serial order. If not so, exchange for the correct Question Paper.

OMR Answer Sheet No. : _____

Registration Number : _____

Name of the Candidate : _____

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web although our aim is to give an understanding of latchup as it occurs in cmos switches similar principles apply to many

other cmos devices latchup may be defined as the creation of a low impedance path between power supply rails as a result of triggering a parasitic device

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web in electronics a latch up is a type of short circuit which can occur in an integrated circuit ic more specifically it is the inadvertent creation of a low impedance path between the power supply rails of a mosfet circuit triggering a parasitic structure which disrupts proper functioning of the part possibly even leading to

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web simply defined latch up is a functional chip failure associated with excessive current going through the chip caused by weak circuit design in some cases latch up can be a temporary condition that can be resolved by power cycle but unfortunately it can also cause a fatal chip failure cmos latch up

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