

Marco Lanzagorta · Stephen Bique
Robert Rosenberg

Introduction to Reconfigurable Supercomputing

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Stephen Bique

Christophe Bobda



Introduction To Reconfigurable Supercomputing Stephen Bique:

Introduction to Reconfigurable Supercomputing Marco Lanzagorta, Stephen Bique, Robert Rosenberg, 2022-05-31 This book covers technologies applications tools languages procedures advantages and disadvantages of reconfigurable supercomputing using Field Programmable Gate Arrays FPGAs The target audience is the community of users of High Performance Computers HPC who may benefit from porting their applications into a reconfigurable environment As such this book is intended to guide the HPC user through the many algorithmic considerations hardware alternatives usability issues programming languages and design tools that need to be understood before embarking on the creation of reconfigurable parallel codes We hope to show that FPGA acceleration based on the exploitation of the data parallelism pipelining and concurrency remains promising in view of the diminishing improvements in traditional processor and system design Table of Contents FPGA Technology Reconfigurable Supercomputing Algorithmic Considerations FPGA Programming Languages Case Study Sorting Alternative Technologies and Concluding Remarks

Space-Time Computing with Temporal Neural Networks James E. Smith, 2022-05-31 Understanding and implementing the brain s computational paradigm is the one true grand challenge facing computer researchers Not only are the brain s computational capabilities far beyond those of conventional computers its energy efficiency is truly remarkable This book written from the perspective of a computer designer and targeted at computer researchers is intended to give both background and lay out a course of action for studying the brain s computational paradigm It contains a mix of concepts and ideas drawn from computational neuroscience combined with those of the author As background relevant biological features are described in terms of their computational and communication properties The brain s neocortex is constructed of massively interconnected neurons that compute and communicate via voltage spikes and a strong argument can be made that precise spike timing is an essential element of the paradigm Drawing from the biological features a mathematics based computational paradigm is constructed The key feature is spiking neurons that perform communication and processing in space time with emphasis on time In these paradigms time is used as a freely available resource for both communication and computation Neuron models are first discussed in general and one is chosen for detailed development Using the model single neuron computation is first explored Neuron inputs are encoded as spike patterns and the neuron is trained to identify input pattern similarities Individual neurons are building blocks for constructing larger ensembles referred to as columns These columns are trained in an unsupervised manner and operate collectively to perform the basic cognitive function of pattern clustering Similar input patterns are mapped to a much smaller set of similar output patterns thereby dividing the input patterns into identifiable clusters Larger cognitive systems are formed by combining columns into a hierarchical architecture These higher level architectures are the subject of ongoing study and progress to date is described in detail in later chapters Simulation plays a major role in model development and the simulation infrastructure developed by the author is described

Deep Learning Systems Andres Rodriguez, 2020-10-26

This book describes deep learning systems the algorithms compilers and processor components to efficiently train and deploy deep learning models for commercial applications The exponential growth in computational power is slowing at a time when the amount of compute consumed by state of the art deep learning DL workloads is rapidly growing Model size serving latency and power constraints are a significant challenge in the deployment of DL models for many applications Therefore it is imperative to codesign algorithms compilers and hardware to accelerate advances in this field with holistic system level and algorithm solutions that improve performance power and efficiency Advancing DL systems generally involves three types of engineers 1 data scientists that utilize and develop DL algorithms in partnership with domain experts such as medical economic or climate scientists 2 hardware designers that develop specialized hardware to accelerate the components in the DL models and 3 performance and compiler engineers that optimize software to run more efficiently on a given hardware Hardware engineers should be aware of the characteristics and components of production and academic models likely to be adopted by industry to guide design decisions impacting future hardware Data scientists should be aware of deployment platform constraints when designing models Performance engineers should support optimizations across diverse models libraries and hardware targets The purpose of this book is to provide a solid understanding of 1 the design training and applications of DL algorithms in industry 2 the compiler techniques to map deep learning code to hardware targets and 3 the critical hardware features that accelerate DL systems This book aims to facilitate co innovation for the advancement of DL systems It is written for engineers working in one or more of these areas who seek to understand the entire system stack in order to better collaborate with engineers working in other parts of the system stack The book details advancements and adoption of DL models in industry explains the training and deployment process describes the essential hardware architectural features needed for today s and future models and details advances in DL compilers to efficiently execute algorithms across various hardware targets Unique in this book is the holistic exposition of the entire DL system stack the emphasis on commercial applications and the practical techniques to design models and accelerate their performance The author is fortunate to work with hardware software data scientist and research teams across many high technology companies with hyperscale data centers These companies employ many of the examples and methods provided throughout the book

Efficient Processing of Deep Neural Networks Vivienne Sze, Yu-Hsin Chen, Tien-Ju Yang, Joel S. Emer, 2020-06-24

This book provides a structured treatment of the key principles and techniques for enabling efficient processing of deep neural networks DNNs DNNs are currently widely used for many artificial intelligence AI applications including computer vision speech recognition and robotics While DNNs deliver state of the art accuracy on many AI tasks it comes at the cost of high computational complexity Therefore techniques that enable efficient processing of deep neural networks to improve metrics such as energy efficiency throughput and latency without sacrificing accuracy or increasing hardware costs are critical to enabling the wide deployment of DNNs in AI systems The book includes background on DNN processing a

description and taxonomy of hardware architectural approaches for designing DNN accelerators key metrics for evaluating and comparing different designs features of the DNN processing that are amenable to hardware algorithm co design to improve energy efficiency and throughput and opportunities for applying new technologies Readers will find a structured introduction to the field as well as a formalization and organization of key concepts from contemporary works that provides insights that may spark new ideas

Performance Analysis and Tuning for General Purpose Graphics Processing Units (GPGPU) Hyesoon Kim, Richard Vuduc, Sara Baghsorkhi, 2012 General purpose graphics processing units GPGPU have emerged as an important class of shared memory parallel processing architectures with widespread deployment in every computer class from high end supercomputers to embedded mobile platforms Relative to more traditional multicore systems of today GPGPUs have distinctly higher degrees of hardware multithreading hundreds of hardware thread contexts vs tens a return to wide vector units several tens vs 1 10 memory architectures that deliver higher peak memory bandwidth hundreds of gigabytes per second vs tens and smaller caches scratchpad memories less than 1 megabyte vs 1 10 megabytes In this book we provide a high level overview of current GPGPU architectures and programming models We review the principles that are used in previous shared memory parallel platforms focusing on recent results in both the theory and practice of parallel algorithms and suggest a connection to GPGPU platforms We aim to provide hints to architects about understanding algorithm aspect to GPGPU We also provide detailed performance analysis and guide optimizations from high level algorithms to low level instruction level optimizations As a case study we use n body particle simulations known as the fast multipole method FMM as an example We also briefly survey the state of the art in GPU performance analysis tools and techniques

Quantum Computer Systems Yongshan Ding, Frederic T. Chong, 2022-05-31 This book targets computer scientists and engineers who are familiar with concepts in classical computer systems but are curious to learn the general architecture of quantum computing systems It gives a concise presentation of this new paradigm of computing from a computer systems point of view without assuming any background in quantum mechanics As such it is divided into two parts The first part of the book provides a gentle overview on the fundamental principles of the quantum theory and their implications for computing The second part is devoted to state of the art research in designing practical quantum programs building a scalable software systems stack and controlling quantum hardware components Most chapters end with a summary and an outlook for future directions This book celebrates the remarkable progress that scientists across disciplines have made in the past decades and reveals what roles computer scientists and engineers can play to enable practical scale quantum computing

Die-stacking Architecture Yuan Xie, Jishen Zhao, 2015-06-01 The emerging three dimensional 3D chip architectures with their intrinsic capability of reducing the wire length promise attractive solutions to reduce the delay of interconnects in future microprocessors 3D memory stacking enables much higher memory bandwidth for future chip multiprocessor design mitigating the memory wall problem In addition heterogenous integration enabled by 3D technology

can also result in innovative designs for future microprocessors This book first provides a brief introduction to this emerging technology and then presents a variety of approaches to designing future 3D microprocessor systems by leveraging the benefits of low latency high bandwidth and heterogeneous integration capability which are offered by 3D technology

Automatic Parallelization Samuel Midkiff,2022-06-01 Compiling for parallelism is a longstanding topic of compiler research This book describes the fundamental principles of compiling regular numerical programs for parallelism We begin with an explanation of analyses that allow a compiler to understand the interaction of data reads and writes in different statements and loop iterations during program execution These analyses include dependence analysis use def analysis and pointer analysis Next we describe how the results of these analyses are used to enable transformations that make loops more amenable to parallelization and discuss transformations that expose parallelism to target shared memory multicore and vector processors We then discuss some problems that arise when parallelizing programs for execution on distributed memory machines Finally we conclude with an overview of solving Diophantine equations and suggestions for further readings in the topics of this book to enable the interested reader to delve deeper into the field Table of Contents Introduction and overview Dependence analysis dependence graphs and alias analysis Program parallelization Transformations to modify and eliminate dependences Transformation of iterative and recursive constructs Compiling for distributed memory machines Solving Diophantine equations A guide to further reading *General-Purpose Graphics Processor Architectures* Tor M. Aamodt,Wilson Wai Lun Fung,Timothy G. Rogers,2018-05-21 Originally developed to support video games graphics processor units GPUs are now increasingly used for general purpose non graphics applications ranging from machine learning to mining of cryptographic currencies GPUs can achieve improved performance and efficiency versus central processing units CPUs by dedicating a larger fraction of hardware resources to computation In addition their general purpose programmability makes contemporary GPUs appealing to software developers in comparison to domain specific accelerators This book provides an introduction to those interested in studying the architecture of GPUs that support general purpose computing It collects together information currently only found among a wide range of disparate sources The authors led development of the GPGPU Sim simulator widely used in academic research on GPU architectures The first chapter of this book describes the basic hardware structure of GPUs and provides a brief overview of their history Chapter 2 provides a summary of GPU programming models relevant to the rest of the book Chapter 3 explores the architecture of GPU compute cores Chapter 4 explores the architecture of the GPU memory system After describing the architecture of existing systems Chapters ref ch03 and ref ch04 provide an overview of related research Chapter 5 summarizes cross cutting research impacting both the compute core and memory system This book should provide a valuable resource for those wishing to understand the architecture of graphics processor units GPUs used for acceleration of general purpose applications and to those who want to obtain an introduction to the rapidly growing body of research exploring how to

improve the architecture of these GPUs

Introduction to Reconfigurable Computing Christophe Bobda, 2007-09-30

Introduction in Reconfigurable Computing provides a comprehensive study of the field Reconfigurable Computing It provides an entry point to the novice willing to move in the research field reconfigurable computing FPGA and system on programmable chip design The book can also be used as teaching reference for a graduate course in computer engineering or as reference to advance electrical and computer engineers It provides a very strong theoretical and practical background to the field of reconfigurable computing from the early Estrin s machine to the very modern architecture like coarse grained reconfigurable device and the embedded logic devices Apart from the introduction and the conclusion the main chapter of the book are the following Architecture of reconfigurable systems which presents the technology and the architecture used in fine grained and those used in coarse grained reconfigurable devices Design and implementation This section deals with the implementation on reconfigurable system It briefly covers the steps needed to implement application on today s FPGAs And focus on the logic synthesis for FPGA in particular LUT technology mapping High Level Synthesis for Reconfigurable Devices The high level synthesis for reconfigurable systems also known as temporal partitioning is presented here Several temporal partitioning techniques are presented and explained Temporal placement This section considers stand alone reconfigurable systems Its assume that a kind of operating systems for reconfigurable systems is in charge of managing the resources of a given system and allocate space on a device for the computation of incoming tasks and therefore presents several temporal placement approaches for off line as well as on line placement On line and Dynamic Interconnection This chapter reviews and explains the different approaches for allowing communication between modules dynamically placed at run time on a given device Designing a reconfigurable application on Xilinx Virtex FPGA In this section the different design approaches of partial reconfigurable systems on the Xilinx FPGAs that are one of the few one on the market with this feature is explained System on programmable chip System on programmable chip is a hot topic in reconfigurable computing This is mainly the integration of a system made upon some peripheral UART Ethernet VGA etc but also computational Coding filter etc hardware modules on one programmable chip The current usable solutions are presented The book furthermore focusses on the development of adaptive multiprocessors on chip i e systems consisting of a set of Processors and exchangeable hardware accelerators Applications This part covers the use of reconfigurable system in computer architecture rapid prototyping reconfigurable supercomputer reconfigurable massively parallel computers and algorithm better adapted for reconfigurable systems distributed arithmetic network packet processing etc

[Introduction to Reconfigurable Computing](#) Christophe Bobda, 2007-11-09 This work is a comprehensive study of the field It provides an entry point to the novice willing to move in the research field reconfigurable computing FPGA and system on programmable chip design The book can also be used as teaching reference for a graduate course in computer engineering or as reference to advance electrical and computer engineers It provides a very strong theoretical and practical background to the field from the early Estrin s

machine to the very modern architecture such as embedded logic devices

Reconfigurable Computing Maya B. Gokhale, Paul S. Graham, 2005-12-14 A one of a kind survey of the field of Reconfigurable Computing Gives a comprehensive introduction to a discipline that offers a 10X 100X acceleration of algorithms over microprocessors Discusses the impact of reconfigurable hardware on a wide range of applications signal and image processing network security bioinformatics and supercomputing Includes the history of the field as well as recent advances Includes an extensive bibliography of primary sources

Reconfigurable Computing Systems Engineering LEV. KIRISCHIAN, 2021-03-31 Reconfigurable Computing Systems Engineering Virtualization of Computing Architecture describes the organization of reconfigurable computing system RCS architecture and discusses the pros and cons of different RCS architecture implementations Providing a solid understanding of RCS technology and where it s most effective this book Details the architecture organization of RCS platforms for application specific workloads Covers the process of the architectural synthesis of hardware components for system on chip SoC for the RCS Explores the virtualization of RCS architecture from the system and on chip levels Presents methodologies for RCS architecture run time integration according to mode of operation and rapid adaptation to changes of multi parametric constraints Includes illustrative examples case studies homework problems and references to important literature A solutions manual is available with qualifying course adoption

Reconfigurable Computing Systems Engineering Virtualization of Computing Architecture offers a complete road map to the synthesis of RCS architecture exposing hardware design engineers system architects and students specializing in designing FPGA based embedded systems to novel concepts in RCS architecture organization and virtualization

A reconfigurable supercomputer architecture W. B. Ligon, Umakishore Ramachandran, Georgia Institute of Technology. School of Information and Computer Science, 1989*

Super Computers V. Rajaraman, 1999 This book explains what a supercomputer is and why such a machine is needed to solve challenging problems in science and engineering The architecture of super computers which distinguishes them from other computers is explained and the need to vectorise programs to make effective use of supercomputers is brought out

Field-Programmable Logic and Applications Manfred Glesner, Peter Zipf, Michel Renovell, 2002-08-21

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